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EXAMINER	
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2618	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/813,327	SUH ET AL.	
	Examiner	Art Unit	
	Andrew Wendell	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *11 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 31, 35-36, 40, 44-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Funk et al. (US Pat# 6,026,119).

Regarding claim 31, Funk et al. wireless packet data communication modem teaches a central processing unit 421 (Fig. 4) operatively connected to a processor bus 432 and 434 (Fig. 4) including address lines and M data lines (Again fig. 5 shows that packet data is being sent through the bus), for processing data received from a plurality of peripherals 425 (Fig. 4) for processing data received from a plurality of peripherals; and a master controller 111 (Fig. 4, Col. 3 lines 26-30) operatively connected to the processor bus including address lines and to a first packet bus 432 and 434 (Fig. 4) having N data lines and to a second packet bus 430 (Fig. 4), for controlling via the first packet bus the plurality of peripherals 425 (Fig. 4), for controlling the signal modulator/demodulator 409 and 417 (Fig. 4) via the second packet bus 430 (Fig. 4).

Regarding claim 35, Funk et al. teaches wherein the master controller controls the plurality of peripherals 101 and 425 (Fig. 4) by issuing a packetized command commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the first

packet bus 432, and 434 (Fig. 4), the packetized command includes a module device select signal used for selecting one of the peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 36, Funk et al. teaches wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of the packetized command (Col. 7 lines 48-54).

Regarding claim 40, Funk et al. teaches controlling a master controller 111 (Fig. 4) via a processor bus 432 (Fig. 4); controlling a plurality of peripherals 425 (Fig. 4) including the signal modulator/demodulator 409 and 417 (Fig. 4) via a common bus 430 (Fig. 4) operatively connected to the master controller and to each of the plurality of peripherals (Col. 3 lines 26-46).

Regarding claim 44, Funk et al. teaches wherein the step of controlling the plurality of peripherals includes issuing a packetized command commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the common bus 430, 432, wherein 434 (Fig. 4), the packetized command includes a module device select signal used for selecting one of the peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 45, Funk et al. teaches wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of the packetized command (Col. 7 lines 48-54).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5-6, 21, and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331).

Regarding claim 1, Funk et al. wireless packet data communication modem teaches a signal modulator/demodulator 409 and 417 (Fig. 4), for effecting radio communications, having an interface operatively connected to a packet bus 430 (Fig. 4) having N data lines for conveying packetized control and data signals (Fig. 5 shows that packet data is sent though the bus to the controller interface); and an application processor having a central processing unit 421 (Fig. 4) operatively connected to a processor bus 432 and 434 (Fig. 4) including address lines and M data lines (Again fig. 5 shows that packet data is being sent through the bus), wherein M is greater than N (it is pretty well known that a logic unit 107 (Fig. 4) is smaller compared to the processor 421 (Fig. 4) unit therefore M is greater than N); and a master controller 111 (Fig. 4, Col. 3 lines 26-30) operatively connected to the processor bus and to the packet bus, for controlling via the packet bus a plurality of peripherals 425 (Fig. 4) operatively connected to the packet bus. Funk et al. fails to clearly teach were M data lines is greater than N data lines even though it pretty well known as explained above.

Dias et al. circuit teaches a control logic unit 1.30 (Fig. 1.2) and a processor 1.14 (Fig. 1.2). It is shown that there are many more M data lines 1.17 (Fig. 1.2) going to the

processor 1.14 (Fig. 1.2) than N data lines 1.22, 1.26, 1.28 (Fig. 1.2) going to the control logic unit 1.30 (Fig. 1.2).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate M data lines is greater than N data lines as taught by Dias et al. into Funk et al. wireless packet data communication modem in order to have a more compact circuit (Col. 7 lines 25-30).

Regarding claim 5, the combination including Funk et al. teaches wherein the master controller controls the plurality of peripherals 101 and 425 (Fig. 4) by issuing a packetized command commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the packet bus 430, 432, and 434 (Fig. 4), wherein the packetized command includes a module device select signal used for selecting one of the plurality of peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 6, the combination including Funk et al. teaches wherein the selected one of the plurality of peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of the packetized command (Col. 7 lines 48-54).

Regarding claim 21, Funk et al. wireless packet data communication modem teaches a central processing unit 421 (Fig. 4) operatively connected to a processor bus 432 and 434 (Fig. 4) including address lines and M data lines (Again fig. 5 shows that packet data is being sent through the bus), for processing data received from a plurality of peripherals 425 (Fig. 4) including a signal modulator/demodulator 409 and 417 for effecting radio communications; and a master controller 111 (Fig. 4, Col. 3 lines 26-30) operatively connected to the processor bus and to a second packet bus having N data

lines 430 (Fig. 4), for controlling via the second bus the plurality of peripherals 425 (Fig. 4) wherein M is greater than N (it is pretty well known that a logic unit 107 (Fig. 4) is smaller compared to the processor 421 (Fig. 4) unit therefore M is greater than N). Funk et al. fails to clearly teach were M data lines is greater than N data lines even though it pretty well known as explained above and a memory shared by the modem and by the central processing unit.

Dias et al. circuit teaches a control logic unit 1.30 (Fig. 1.2) and a processor 1.14 (Fig. 1.2). It is shown that there are many more M data lines 1.17 (Fig. 1.2) going to the processor 1.14 (Fig. 1.2) than N data lines 1.22, 1.26, 1.28 (Fig. 1.2) going to the control logic unit 1.30 (Fig. 1.2).

Regarding claim 25, Funk et al. further teaches wherein the master controller controls the plurality of peripherals 101 and 425 (Fig. 4) by issuing a packetized command commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the common bus 430, 432, and 434 (Fig. 4), wherein the packetized command includes a module device select signal used for selecting one of the peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 26, Funk et al. further teaches wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of the packetized command (Col. 7 lines 48-54).

3. Claims 2-3, 7, 11-12, 14-16, 18, 22-23, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331) and further in view of Gibbs et al. (US Pat Appl# 2003/0114152).

Regarding claim 2, Funk et al. wireless packet data communication modem and Dias et al. circuit teaches the limitations in claim 1. Funk et al. and Dias et al. fails to teach about a memory shared by the modem and the master controller.

Gibbs et al. wireless trickle sync device teaches a shared memory 30 (Fig. 1) operatively connected to the modem 50 (Fig. 1) and the master controller 20 (Fig. 1) for access by either the modem 50 (Fig. 1) or the central processing unit 40 (Fig. 1).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a memory shared by the modem and the master controller as taught by Gibbs et al. into M data lines is greater than N data lines as taught by Funk et al. in view of Dias et al. circuit in order to reduce power consumption (Section 0002).

Regarding claim 3, Funk et al. further teaches it would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate SDRAM memory into Funk et al. memory in order to provide small size, light weight, and low costs (Col. 2 lines 29-33).

Regarding claim 7, Gibbs et al. further teaches wherein the packetized command includes a read/write command (SRAM, Section 0013) to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the AP 40 (Fig. 1).

Regarding claim 11, Funk et al. wireless packet data communication modem teaches a signal modulator/demodulator 409 and 417 (Fig. 4), for effecting radio

communications, having an interface operatively connected to a packet bus 430 (Fig. 4) having N data lines for conveying packetized control and data signals (Fig. 5 shows that packet data is sent though the bus to the controller interface); and a central processing unit 421 (Fig. 4) operatively connected to a processor bus 432 and 434 (Fig. 4) including address lines and M data lines (Again fig. 5 shows that packet data is being sent through the bus), wherein M is greater than N (it is pretty well known that a logic unit 107 (Fig. 4) is smaller compared to the processor 421 (Fig. 4) unit therefore M is greater than N); and a master controller 111 (Fig. 4, Col. 3 lines 26-30) operatively connected to the processor bus and to a first packet bus having N data lines 430 (Fig. 4) and to the second packet bus 432 (Fig. 4), for controlling via the first packet bus at least one peripheral 425 (Fig. 4) and via the second packet bus 432 (Fig. 4) a memory 419 (Fig. 4) shared by the modem and by the central processing unit. Funk et al. fails to clearly teach were M data lines is greater than N data lines even though it pretty well known as explained above and a memory shared by the modem and by the central processing unit.

Dias et al. circuit teaches a control logic unit 1.30 (Fig. 1.2) and a processor 1.14 (Fig. 1.2). It is shown that there are many more M data lines 1.17 (Fig. 1.2) going to the processor 1.14 (Fig. 1.2) than N data lines 1.22, 1.26, 1.28 (Fig. 1.2) going to the control logic unit 1.30 (Fig. 1.2).

Funk et al. and Dias et al. fail to teach via a second bus a memory shared by the modem and the AP.

Gibbs et al. wireless trickle sync device teaches a second bus a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the central processing unit 40 (Fig. 1).

Regarding claim 12, Gibbs et al. further teaches wherein the master controller further controls via the second bus a flash memory (Section 0013).

Regarding claim 14, Funk et al. further teaches wherein the master controller controls the plurality of peripherals 101 and 425 (Fig. 4) operatively connected to first packet bus by issuing a packetized command commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the first packet bus 430 (Fig. 4), the packetized command includes a module device select signal used for selecting one of the peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 15, Funk et al. further teaches wherein the selected one of the plurality of peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of command (Col. 7 lines 48-54).

Regarding claim 16, Gibbs et al. further teaches wherein the packetized command includes a read/write command (SRAM, Section 0013) to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the central processing unit 40 (Fig. 1).

Regarding claim 18, it would have been obvious to use SDRAM as a possible choice for memory because of its size and performance (see claim 3).

Regarding claim 22, Gibbs et al. further teaches a shared memory 30 (Fig. 1) operatively connected to the modem 50 (Fig. 1) and the master controller 20 (Fig. 1) for access by either the modem 50 (Fig. 1) or the central processing unit 40 (Fig. 1).

Regarding claim 23, it would have been obvious to use SDRAM as a possible choice for memory because of its size and performance (Claim 3).

Regarding claim 27, Gibbs et al. further teaches wherein the packetized command includes a read/write command (SRAM, Section 0013) to the memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and by the central processing unit 40 (Fig. 1).

4. Claims 4 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331) and further in view of Wilska et al. (US Pat Appl# 2002/0082043).

Regarding claim 4, Funk et al. wireless packet data communication modem in view of Dias et al. circuit teaches the limitations in claim 1 and wherein the plurality of peripherals include at least one of an a display 425 (Fig. 4) of Funk et al. reference. Funk et al. and Dias et al. fails to teach a plurality of peripherals include at least one of an image capture module and a flash memory.

Wilska et al. device for personal communications teaches wherein the plurality of peripherals operatively connected to the bus include the modem 17 (Fig. 3) and at least one of an image capture module 14 (Fig. 3), a display 9 (Fig. 3), and a flash memory 13 (Fig. 3).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a plurality of peripherals include at least one of an image capture module and a flash memory as taught by Wilska et al. into M data lines is greater than N data lines as taught by Funk et

al. in view of Dias et al. circuit in order to collect data efficiently and to communicate with the environment (Section 0005).

Regarding claim 24, Wilska et al. further teaches wherein the plurality of peripherals additionally include at least one of an image capture module 14 (Fig. 3), a display 9 (Fig. 3), and a flash memory 13 (Fig. 3).

5. Claims 8-9, 17, 19, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331) further in view of Gibbs et al. (US Pat Appl# 2003/0114152) and further Watanabe et al. (US Pat# 6,378,102).

Regarding claim 8, Funk et al. wireless packet data communication modem in view of Dias et al. circuit and further in view of Gibbs et al. wireless trickle sync device teaches the limitations in claims 1, 5, and 7. Funk et al., Dias et al. and Gibbs et al. fail to teach about a strobe signal.

Watanabe et al. synchronous semiconductor memory device with multi-bank configuration teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a strobe signal as taught by Watanabe et al. into a memory shared by the modem and the master controller as taught by Gibbs et al. into M data lines is greater than N data lines as

taught by Funk et al. in view of Dias et al. circuit in order to have faster operation (Col. 2 lines 4-10).

Regarding claim 9, Watanabe et al. further teaches wherein the SDRAM includes a plurality of data banks (Col. 2 lines 20-24) and an interface for interfacing the master controller (Col. 26 lines 1-6).

Regarding claim 17, Watanabe et al. further teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Regarding claim 19, Watanabe et al. further teaches wherein the SDRAM includes a plurality of data banks (Col. 2 lines 20-24) and an interface for interfacing the master controller via the second bus (Col. 26 lines 1-6).

Regarding claim 28, Watanabe et al. further teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Regarding claim 29, Watanabe et al. further teaches wherein the SDRAM includes a plurality of data banks (Col. 2 lines 20-24) and an interface for interfacing the master controller (Col. 26 lines 1-6).

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331) further in view of Gibbs et al. (US Pat Appl# 2003/0114152) and further Fueki (US Pat Appl# 2002/0166058).

Regarding claim 10, Funk et al. wireless packet data communication modem in view of Dias et al. circuit and further in view of Gibbs et al. wireless trickle sync device teaches the limitations in claims 1, 2, and 3. Funk et al., Dias et al. and Gibbs et al. fail to teach a protection signal.

Fueki's semiconductor integrated circuit on IC card protected against tampering teaches wherein the memory includes a protection circuit for receiving address data from an external devices and for generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a protection signal as taught by Fueki into a memory shared by the modem and the master controller as taught by Gibbs et al. into M data lines is greater than N data lines as taught by Funk et al. in view of Dias et al. circuit in order to increase security (section 0015).

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331) and further in view of Gibbs et al. (US Pat Appl# 2003/0114152) as applied to claim 11 above, and further in view of Wilska et al. (US Pat Appl# 2002/0082043).

Regarding claim 13, Funk et al. in view of Dias et al. and further in view of Gibbs et al. teaches the limitations in claim 11. Funk et al., Dias et al., and Gibbs et al. fail to teach an image capture module.

Wilska et al. device for personal communications teaches wherein the at least one peripheral is an image capture module 14 (Fig. 3).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate an image capture module as taught by Wilska et al. into a memory shared by the modem and the master controller as taught by Gibbs et al. into M data lines is greater than N data lines as taught by Funk et al. in view of Dias et al. circuit in order to collect data efficiently and to communicate with the environment (Section 0005).

8. Claims 20 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331) and further in view of Gibbs et al. (US Pat Appl# 2003/0114152) as applied to claims 11 and 18 above, and further in view of Fueki (US Pat Appl# 2002/0166058).

Regarding claim 20, Funk et al. in view of Dias et al. and further in view of Gibbs et al. teaches the limitations in claims 11 and 18. Funk et al., Dias et al., and Gibbs et al. fail to teach a protection signal.

Fueki's semiconductor integrated circuit on IC card protected against tampering teaches wherein the memory includes a protection circuit for receiving address data from an external devices and for generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a protection signal as taught by Fueki into a memory shared by the modem and the master controller as taught by Gibbs et al. into M data lines is greater than N data lines as taught by Funk et al. in view of Dias et al. circuit in order to increase security (section 0015).

Regarding claim 30, Fueki further teaches wherein the memory includes a protection circuit for receiving address data from an external devices and for generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

9. Claims 32-33, 37, 41, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Gibbs et al. (US Pat Appl# 2003/0114152).

Regarding claim 32, Funk et al. wireless packet data communication modem teaches the limitations in claim 31. Funk et al. fails to teach about a memory shared by the modem and the central processing unit.

Gibbs et al. wireless trickle sync device teaches a memory 30 (Fig. 1) shared by the modem 50 (Fig.1) and the central processing unit 40 (Fig. 1).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a memory shared by the modem and the central processing unit as taught by Gibbs et al. into Funk et al. circuit in order to reduce power consumption (Section 0002).

Regarding claim 33, the combination including Funk et al. teaches it would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate SDRAM

memory into Funk et al. memory in order to provide small size, light weight, and low costs (Col. 2 lines 29-33).

Regarding claim 37, the combination including Gibbs et al. teaches wherein the packetized command includes a read/write command (SRAM, Section 0013) to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the central processing unit 40 (Fig. 1).

Regarding claim 41, the combination including Gibbs et al. teaches about a memory 30 (Fig. 1) shared by the modem 50 (Fig.1) and the central processing unit 40 (Fig. 1).

Regarding claim 46, the combination including Gibbs et al. teaches wherein the packetized command includes a read/write command (SRAM, Section 0013) to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the central processing unit 40 (Fig. 1).

10. Claims 34 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Wilska et al. (US Pat Appl# 2002/0082043).

Regarding claim 34, Funk et al. wireless packet data communication modem teaches the limitations in claim 31 and wherein the plurality of peripherals include at least one of an a display 425 (Fig. 4) connected to the first packet bus. Funk et al. fails to teach a plurality of peripherals include at least one of an image capture module and a flash memory.

Wilska et al. device for personal communications teaches wherein the plurality of peripherals include at least one of an image capture module 14 (Fig. 3), a display 9 (Fig. 3), and a flash memory 13 (Fig. 3).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a plurality of peripherals include at least one of an image capture module and a flash memory as taught by Wilska et al. into Funk et al. circuit in order to collect data efficiently and to communicate with the environment (Section 0005).

Regarding claim 43, Wilska et al. teaches wherein the plurality of peripherals include at least one of an image capture module 14 (Fig. 3), a display 9 (Fig. 3), and a flash memory 13 (Fig. 3).

11. Claims 38-39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Gibbs et al. (US Pat Appl# 2003/0114152) as applied to claims 31, 35, and 37 above, and further in view of Watanabe et al. (US Pat# 6,378,102).

Regarding claim 38, the combination of Funk et al. in view of Gibbs et al. teaches the limitations in claims 31, 35, and 37. Funk et al. and Gibbs et al. both fail to teach about a strobe signal.

Watanabe et al. synchronous semiconductor memory device with multi-bank configuration teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a strobe signal as taught by Watanabe et al. into a memory shared by the modem and the AP as taught by Gibbs et al. into Funk et al. circuit in order to have faster operation (Col. 2 lines 4-10).

Regarding claim 39, the combination including Watanabe et al. teaches wherein the SDRAM includes a plurality of data banks (Col. 2 lines 20-24) and an interface for interfacing the master controller (Col. 26 lines 1-6).

12. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119).

Regarding claim 42, Funk et al. wireless packet data communication modem teaches the limitations in claim 40. Funk et al. fails to teach about shared memory of being SDRAM.

It would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate SDRAM memory into Funk et al. memory in order to provide small size, light weight, and low costs (Col. 2 lines 29-33).

13. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Watanabe et al. (US Pat# 6,378,102).

Regarding claim 47, Funk et al. Funk et al. wireless packet data communication modem teaches the limitations in claim 40. Funk et al. fails to teach about a strobe signal.

Watanabe et al. synchronous semiconductor memory device with multi-bank configuration teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a strobe signal as taught by Watanabe et al. into Funk et al. circuit in order to have faster operation (Col. 2 lines 4-10).

14. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Gibbs et al. (US Pat Appl# 2003/0114152) as applied to claims 40 and 41 above, and further in view of Fueki (US Pat Appl# 2002/0166058).

Regarding claim 48, the combination of Funk et al. in view of Gibbs et al. teaches the limitations in claims 40 and 41. Funk et al. and Gibbs et al. both fail to teach a protection signal.

Fueki's semiconductor integrated circuit on IC card protected against tampering teaches wherein the memory includes a protection circuit for receiving address data from an external devices and for generating a protect signal upon simultaneously receiving the same address from external devices (Sections 0014 and 0031).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a protection signal as taught by Fueki into a memory shared by the modem and the AP as taught by Gibbs et al. into Funk et al. circuit in order to increase security (section 0015).

Response to Arguments

Applicant's Remarks	Examiner's Response
Regarding claim 40, "Funk arguably teaches a second peripheral on a third bus shown as directly connected to the processor, but not through any "master controller" 111."	Controller interface 111 (Fig. 4) is a master controller because it is used to control information and provide other services (Col. 3 lines 26-30). Even though it is not called a master controller, it does the same functions as claimed.
Regarding claim 40, "Further, Funk does not teach both the first peripheral and the second peripheral being on the same "common bus" and being controlled by a "master controller."	Applicant may be right, however the claim language does not indicate the first and second peripheral being connected to a bus. The claim reads the bus being **operatively** connected to the master controller. The term operatively does not mean being on the same bus.

15. Applicant's arguments with respect to claims 1-39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Wendell whose telephone number is 571-272-0557. The examiner can normally be reached on 7:30-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on 571-272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Wendell

Andrew Wendell
Examiner
Art Unit 2618

5/5/2005

NAY MAUNG
SUPERVISORY PATENT EXAMINER